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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,951	04/02/2004	Greg A. Blodgett	M4065.0285/P285-C	8919

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EXAMINER	
NGUYEN, TAN	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,951	BLODGETT, GREG A.	
	Examiner	Art Unit	
	Tan T. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *56-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *58* is/are allowed.

6)☒ Claim(s) *56,57,64-66 and 74* is/are rejected.

7)☐ Claim(s) *59-63, 67-73, 75-77* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following action is in response to the amendment filed by Applicants on November 3, 2004.

2. New claims 74-77 have been added

Claims 56-73 have been added.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 56-57, 64-66 and 74 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 52-54 of U.S. Patent No. 6,327,178. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 53 of U.S. Patent No. 6,327,178 recited a method of operating a programmable circuit comprising the step of causing a gate threshold voltage level of a permanently programmable transistor to be at one of a first gate threshold voltage value and a second gate threshold voltage value by applying predetermined voltages to gate and drain terminals of the programmable transistor to change the gate threshold voltage from one of the first and second threshold voltages to the other of the first and second gate threshold voltage, wherein the causing step

includes programming the programmable transistor by applying predetermined voltages to gate and drain terminals of the programmable transistor (claim 54); and determining an operative state of the programmable transistor during a time when the transistor is biased for operation and a third gate threshold voltage, between the first and second threshold voltage values, is applied to a gate of the programmable transistor when the third threshold voltage is applied, wherein the determining step occurs in response to the occurrence of a read signal (claim 52).

It would have been obvious to a person of ordinary skill in the art to use the programmable transistor in claims 52-54 of U.S. Patent No. 6,327,178 as the claimed transistor disposed in the memory device in claim 56 of the present application.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to use the programmable transistor of claims 52-54 of U.S. Patent No. 6,327,178 as the transistor in the memory device to store data whose states corresponding to the threshold voltage values of the programmable transistor.

Regarding claims 65-66, claim 54 of U.S. Patent No. 6,327,178 recited the predetermined voltages are applied to gate and drains terminals of the programmable, which inherently includes different voltages are applied on different signal lines to the gate and drain terminals.

Regarding claims 57 and 74, claim 1 of U.S. Patent No. 6,327,178 recited a read circuit for reading the program status of the programmable transistor for applying voltage to source and drain terminals of the programmable transistor and a third

threshold voltage which is between the first and second threshold voltages to the gate of the programmable transistor.

Claim 1 and claim 52 of U.S. Patent 6,327,178 did not disclose the steps of reading the conductivity state of the transistor and perceiving an identity of the memory device according to the conductivity state as claimed in claim 57 of the present application.

It is old and well known in the art that the state of a memory cell would be determined by sensing the conductivity of the current through the transistor.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify claim 1 and claim 52 of U.S. Patent No. 6,327,178 by adding the step of sensing the current of the transistor.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to sense the flow of current through the transistor to accurately determine the state of the data stored in the transistor.

Regarding claim 64, claim 1 and claim 52-54 of U.S. Patent No. 6,327,178 did not disclose the "ON" and "OFF" states of the transistor. It is inherent that as the amount of charge being stored in the gate of the transistor affects the flow of the current conductivity of the transistor which indicates the "ON" and "OFF" states of the transistor.

5. Claims 59-63, 67-73, 75-77 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Applicant's arguments with respect to claims 56-57, 59, 61-62, 64-67, 69-72 have been considered but are moot in view of the new ground(s) of rejection.

7. REMARKS

8. Regarding claims 56-57, Applicants asserted in the REMARKS (page 7, last paragraph" that Wang (U.S. Patent No. 6,330,190) does not teach or suggest "applying a read voltage to a gate of said transistor, wherein said read voltage is between said first value and said second value". In light of Applicants' argument, an obviousness-type double patenting rejection to claims 56-57, 64-66 and 74 based on claims 1, 52-54 of U.S. Patent No. 6,327,178 have been made. Claims 52-54 of U.S. Patent No. 6,327,178 recited a method of operating a programmable circuit comprising the step of causing a gate threshold voltage level of a permanently programmable transistor to be at one of a first gate threshold voltage value and a second gate threshold voltage value by applying predetermined voltages to gate and drain terminals of the programmable transistor to change the gate threshold voltage from one of the first and second threshold voltages to the other of the first and second gate threshold voltage, wherein the causing step includes programming the programmable transistor by applying predetermined voltages to gate and drain terminals of the programmable transistor (claim 54); and determining an operative state of the programmable transistor during a time when the transistor is biased for operation and a third gate threshold voltage, between the first and second threshold voltage values, is applied to a gate of the programmable transistor when the third threshold voltage is applied, wherein the determining step occurs in response to the occurrence of a read signal (claim 52).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday To Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached at (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2818
November 22, 2004